Claims

1. A cold cathode type flat panel display comprising:

a first substrate including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode, an upper electrode and an electron acceleration layer retained between said lower electrode and said upper electrode, each of said thin-film type electron sources emitting electrons from said upper electrode in response to a voltage applied between said lower electrode and said upper electrode; and

a second substrate including a fluorescent screen in which a plurality of phosphors to be excited by said electrons emitted from said first substrate are arrayed;

said cold cathode type flat panel display being characterized in that each of said arrays of said thin-film type electron sources includes a first interlayer insulation layer and an upper electrode feeder wiring serving as a power feed line to said upper electrode; and

a second interlayer insulation layer is provided between said electron acceleration layer and said upper electrode.

2. A cold cathode type flat panel display according to Claim 1, characterized in that:

said lower electrode is made of aluminum or an aluminum alloy;

said electron acceleration layer and said first interlayer insulation layer are anodic oxide films of said aluminum or aluminum alloy forming said lower electrode; and

said second interlayer insulation layer is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films of said aluminum or aluminum alloy forming said lower electrode.

3. A cold cathode type flat panel display according to Claim 2, characterized in that:

a terminal portion of said second interlayer insulation layer surrounding an electron acceleration region has a normal dip shape.

4. A cold cathode type flat panel display according to Claim 2, characterized in that:

said second interlayer insulation layer has a structure of a plurality of layers; and

said second interlayer insulation layer has a normal dip shape in a terminal portion thereof surrounding an electron emission region, said normal dip shape being formed using a difference in etching rate among said layers.

5. A cold cathode type flat panel display comprising a substrate and a fluorescent screen, said substrate including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode, an upper electrode and an electron acceleration layer retained between said lower electrode and said upper electrode, each of said thin-film type electron sources emitting electrons from said upper electrode in response to a voltage applied between said lower electrode and said upper electrode;

said cold cathode type flat panel display being characterized in that:

each of said arrays of said thin-film type electron sources includes a first interlayer insulation layer and an upper electrode feeder wiring serving as a power feed line to said upper electrode; and

a region for emitting electrons is surrounded by a second interlayer insulation layer put between said electron acceleration layer and said upper electrode.

6. A cold cathode type flat panel display according to Claim 5, characterized in that:

said lower electrode is made of aluminum or an aluminum alloy, while said electron acceleration layer and said first

interlayer insulation layer are anodic oxide films of said aluminum or aluminum alloy; and

said second interlayer insulation layer is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films.

7. A cold cathode type flat panel display according to Claim 5, characterized in that:

a terminal portion of said second interlayer insulation layer surrounding said electron emission region has a normal dip shape.

8. A cold cathode type flat panel display according to Claim 5, characterized in that:

said second interlayer insulation layer has a structure of a plurality of layers; and

said second interlayer insulation layer has a normal dip shape in a terminal portion thereof surrounding said electron emission region, said normal dip shape being formed using a difference in etching rate among said layers.

[FIG. 4]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 5]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 6]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 7]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 8]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 9]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 10]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 11]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 12]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 13]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 14]

(a) CHEMICAL CONVERSION CURRENT (ANY UNIT)

WITH SECOND INTERLAYER INSULATION LAYER

OXIDIZATION TIME (MINUTE)

(b) CHEMICAL CONVERSION CURRENT (ANY UNIT)

WITHOUT SECOND INTERLAYER INSULATION LAYER

OXIDIZATION TIME (MINUTE)

[FIG. 16]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 17]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 18]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 19]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 20]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 21]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 22]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 23]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 24]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 25]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 26]

EMBODIMENT 1

EMBODIMENT 2

OPERATION TIME (khr)

[FIG. 27]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 28]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 29]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 30]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 31]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 32]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 33]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 34]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 35]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 36]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 37]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 38]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 39]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 40]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 41]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 42]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 43]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 44]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 45]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 48]

TIME

[FIG. 50]

A-A' SECTION

B-B' SECTION

[FIG. 51]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 52]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 53]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 54]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 55]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 56]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 57]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 58]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 59]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 60]

(a) A-A' SECTION

(b) B-B' SECTION

[FIG. 61]

(b) A-A' SECTION

(c) B-B' SECTION

[FIG. 62]

(a) A-A' SECTION

(b) B-B' SECTION